Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SUNIL D. MEHTA

Appeal No. 1999-2683
Application 08/754,564[1]

ON BRIEF

Before BARRETT, GROSS, and BLANKENSHIP, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 18-32. Claims 1-17 have been

[1] Application for patent filed November 21, 1996, entitled "Borderless Vias On Bottom Metal."

withdrawn pursuant to a restriction requirement. The amendment (Paper No. 17) filed February 16, 1999, has not been entered.

We reverse.

BACKGROUND

The invention relates to an integrated circuit, claimed in structural and product-by-process format, having an etch stop layer on top of the bottom metal lines and under the interlayer dielectric (ILD) to prevent overetching during via formation. Overetching can cause exploding misaligned vias and trenching.

Claim 18 is reproduced below.

> 18. An integrated circuit having a plurality of semiconductor devices therein and a multilevel metallization structure for interconnection of said semiconductor devices thereon, said multilevel metallization structure comprising:
>
> a plurality of substantially parallel, separated, patterned metal layers including a first bottom metal layer and a second top metal layer, said first bottom metal layer being separated from said top metal layer by an ILD layer therebetween, each of said patterned metal layers being comprised of metal lines separated by gaps;
>
> said ILD layer between said first bottom metal layer and said second top metal layer having vias therethrough, said vias having conducting via plugs therein, said via plugs providing electrical connectivity between said first metal bottom layer and said top metal layer;

> said bottom metal layer having therein at least one bottom metal line having a top conducting surface and an edge surface, said bottom metal line being surrounded by a dielectric layer having a top dielectric surface, said top conducting surface and said top dielectric surface being substantially locally coplanar near said bottom metal line, a first portion of said top dielectric surface not being coincident with said vias, and a first portion of said top conducting metal surface not being coincident with said vias;
>
> said first portion of said top dielectric surface not coincident and said first portion of said top conducting metal surface not coincident having thereon a thin non-conducting via etch-stop layer under said ILD.

The Examiner relies on the admitted prior art (APA) of Appellant's figures 1 and 4 and following references:

Tsu	5,432,128	July 11, 1995
Kalnitsky (European Patent Application)	EP 0 523 856	January 20, 1993

Claims 18-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsu, Kalnitsky, and the APA. The Examiner finds that Tsu discloses the structure of independent claim 18 except "that it does not specifically disclose that a thin oxide layer 24 in Fig. 3f is an etch-stop layer of silicon nitride" (Final Rejection, p. 3). However, the Examiner finds that silicon oxide layer 24 of Tsu is clearly

used as an etch stop layer because it was well known that the overlying SOG is softer and has a higher etching rate than silicon oxide. The Examiner finds that Tsu suggests (at col. 3, element 24 in Table 1) that other dielectric materials can be substituted for layer 24. The Examiner concludes that it would have been obvious to substitute a silicon nitride etch stop layer as taught by Kalnitsky for the silicon oxide layer 24 in Tsu "because the silicon nitride layer also has lower etching rate than the SOG layer, and because it could be used as an etch stop layer to protect damaging interaction with chemicals associated with subsequent process steps, such as explicitly taught by Kalnitsky (column 2, lines 14-19)" (Final Rejection, p. 4). The Examiner finds that neither Tsu nor Kalnitsky discloses a plurality of substantially parallel, separated, patterned metal layers, but finds that such limitation is taught in the APA of Appellant's figure 1 and concludes that it would have been obvious to construct a plurality of layers in Tsu in view of the APA (Final Rejection, p. 4). The Examiner interprets independent claim 26 as a product-by-process claim and impliedly concludes

that the product would have been obvious over the combination of Tsu, Kalnitsky, and the APA (Final Rejection, pp. 4-5).

We refer to the final rejection (Paper No. 11) (pages referred to as "FR__") and the examiner's answer (Paper No. 21) (pages referred to as "EA__") for a statement of the Examiner's position, and to the appeal brief (Paper No. 20) for a statement of Appellant's arguments thereagainst.

OPINION

Arguments

The Examiner finds that oxide layer 24 in Tsu is inherently an etch stop layer for the overlying spin-on-glass (SOG) layer 26 and concludes that it would have been obvious to substitute a silicon nitride etch stop layer as taught by Kalnitsky.

Appellant argues that CVD oxide layer 24 in Tsu is not stated to be an etch stop layer and could not be effectively used as an etch stop layer. Appellant provides a declaration by the inventor Sunil Mehta under 37 CFR § 1.132 (Paper No. 10) which states (p. 2):

> 4. To the best of my knowledge on information and belief, the industry accepted definition of an etch stop layer is a layer of material underlying the material being etched and having a lower etch rate than the

> overlying material being etched, its etch rate being sufficiently lower so that the etch stop layer is substantially unaffected during any necessary overetch.

Appellant also provides an addendum to the declaration of Mr. Mehta (Paper No. 16) which states that "the relative etch rate difference between CVD oxide [layer 24] and SOG [layer 26 in Tsu] is approximately 2:1 or less" (para. 5) based on U.S. Patent 5,173,151, issued December 22, 1992, to Namose, which was cited by the Examiner. Mr. Mehta further declares (para. 6):

> 6. To the best of my knowledge on information and belief, for both the structures in Tsu and in the present invention, a minimum etch rate difference of 4:1 between the ILD and the underlying layer is required to effectively use the underlying layer as a via etch stop layer. It is well known in the art that standard dry etch processes provide an etch rate selectivity of at least 4:1 for silicon dioxide over silicon nitride.

Mr. Mehta also states (para. 7) that it was well known in the art to use CVD layers (such as CVD oxide layer 24 in Tsu) as chemical barriers to prevent contact between SOG and materials such as resist and metal, citing the reference by Chu et al. (Chu), Spin-on-Glass Dielectric Planarization for Double Metal CMOS Technology, Proc. 1986 VMIC Conference, pp. 474-483.

Appellant explains that it is necessary to overetch, that is, to employ an etch for a period longer than the calculated

time to etch a given thickness, to accommodate variable thickness and etch rate non-uniformity to ensure complete removal of material (Br6) and since oxide layer 24 in Tsu is not specified to be an etch stop, it would not have an etch selectivity high enough to remain unaffected during via overetch (Br8).

Analysis

The problem of oxide overetch in making borderless (unframed) contacts or vias was known in the prior art, as was the general solution of using "etch stop" dielectrics to prevent the etching from undercutting the underlying metal pattern. See Pimbley et al., VLSI Electronics Microstructure Science - Vol. 19,(Academic Press, Inc. 1989), pp. 74, 95; Jang et al., U.S. Patent 5,840,624, issued November 24, 1998, filed March 15, 1996 (copies attached). The secondary reference to Kalnitsky addresses the problem of overetching and is arguably a much stronger reference than Tsu. However, the Examiner has elected to use as a primary reference the Tsu patent which does not address the problems of misaligned vias or overetching. We address the rejection as stated by the Examiner, rather than some rejection we could create out of

the references, to avoid making a new ground of rejection. See In re Kronig, 539 F.2d 1300, 1302, 190 USPQ 425, 426 (CCPA 1976) (the "ultimate criterion" of whether a rejection is new is "whether appellants have had a fair opportunity to react to the thrust of the rejection").

There are at least two problems with the Examiner's rejection. First, we find that the CVD oxide layer 24 in Tsu is not inherently an etch stop layer. Tsu does not expressly or impliedly disclose the oxide layer 24 to be an etch stop layer. Although statements by an inventor may be entitled to less weight because they can be self-serving, we are persuaded by the declarations of Mr. Mehta and the arguments that the oxide layer 24 would not necessarily function as an etch stop layer during overetching. Mr. Mehta has provided a reference to Chu showing that CVD oxide layers are known to serve a function in the prior art unrelated to the etch stop function; thus, one skilled in the art would not assume layer 24 is an etch stop layer. Mr. Mehta states that there is at most a 2:1 etch rate difference between the CVD oxide layer 24 and the SOG layer 26, which is less than the 4:1 ratio one skilled in the art would consider to be an etch stop layer. While we

understand the Examiner's position that layer 24 could function as an etch stop layer because of this small relative etch rate difference, we find it would not necessarily serve this function unless one of ordinary skill in the art recognized that layer 24 should function as an etch stop layer so that the amount of overetch could be controlled to prevent etching through the thin layer 24. Inherency requires that a characteristic or property necessarily be in the prior art reference. See In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (the mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency). The initial burden of establishing a prima facie case of inherency by evidence or persuasive reasoning is on the examiner, after which the burden shifts to appellant. See In re Schreiber, 128 F.3d 1473, 1478, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997). In addition, "[i]n order to render a claimed apparatus or method obvious, the prior art must enable one skilled in the art to make and use the apparatus or method." Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 1471, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997). That is, the prior art

must teach the invention. Since there is no evidence that one of ordinary skill in the art was aware that the layer 24 should function as an etch stop layer, it cannot be said that the prior art enables those of ordinary skill in the art to make a semiconductor device with an etch stop layer.

Second, we find no motivation for one of ordinary skill in the art to modify Tsu to have a silicon nitride etch stop layer as taught in Kalnitsky. Lack of motivation may preclude a prima facie case of obviousness. The Examiner modifies the material of layer 24 based on an etch stop property that is not known, but that the Examiner considers inherent. This modification based on an unknown, but inherent property (assuming it were so) is not proper. See In re Spormann, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966) ("That which may be inherent is not necessarily known. Obviousness cannot be predicated on what is unknown."). If one skilled in the art did not recognize that the layer 24 in Tsu should be an etch stop layer, he or she would not have been motivated to substitute a real etch stop layer, such as the silicon nitride layer of Kalnitsky. As to the Examiner's finding that one of ordinary skill in the art would have been motivated to arrive

at the claimed subject matter by substituting other dielectric materials in Tsu including the silicon nitride of Kalnitsky (FR3), this is essentially a statement that the claimed subject matter could be arrived at by luck or hindsight, which is not proper motivation. We agree with Appellant's argument (Br7) that because all of the alternate materials in Table 1 of Tsu are oxides, and the generic term for layer 24 is "thin oxide layer," Tsu teaches away from the use of silicon nitride for layer 24.

For the reasons stated above, we conclude that the Examiner has failed to state a prima facie case of obviousness over Tsu in view of Kalnitsky and the APA as to independent claims 18 and 26. Accordingly, the rejection of claims 18-32 is reversed.

In the Response to Argument section of the examiner's answer, it appears that the Examiner tries to shift the rejection to apply Kalnitsky alone or in combination with the APA (e.g., EA9-10). This is not the stated rejection and the Examiner cannot twist the rejection around to a new ground of rejection by arguments made for the first time only in the remarks. Kalnitsky is a very good reference and we think it

should have been the primary reference since, unlike Tsu, it deals with Appellant's problem of overetching and teaches an etch stop layer 38. However, Appellant points out (Br9) that Kalnitsky alone is not sufficient to meet the claims because Kalnitsky has a conformal oxide layer 20 directly and contiguously atop metal line 16 and beneath nitride layer 38. Claim 18 requires "said top conducting metal surface . . . having thereon a thin non-conducting via etch-stop layer under said ILD" and claim 26 requires "depositing a non-conducting via etch stop layer onto said top conducting surface of said bottom metal line," which we interpret to require the etch stop layer to be in direct contact with the top conducting surface. The Examiner does not address this difference and we decline to enter a new ground of rejection without knowing the Examiner's views or whether the Examiner could find prior art to address this difference. Accordingly, we have only addressed the stated ground of rejection.

CONCLUSION

The rejection of claims 18-32 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)	
ANITA PELLMAN GROSS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)	

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